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October 1995 Revised August 2004

NC7S86

TinyLogic® HS 2-Input Exclusive-OR Gate

General Description

The NC7S86 is a single 2-Input high performance CMOS Exclusive-OR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. Inputs are well buffered from the output to assure high noise immunity and reduced sensitivity to input edge rate.

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed; t_{PD} 4.5 ns typ
- \blacksquare Low Quiescent Power; I_CC < 1 μA
- Balanced Output Drive; 2 mA I_{OL}, -2 mA I_{OH}
- Broad V_{CC} Operating Range; 2V–6V
- Balanced Propagation Delays
- Specified for 3V operation

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7S86M5X	MA05B	7S86	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7S86P5X	MAA05A	S86	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7S86L6X	MAC06A	ZZ	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol



Pin Descriptions

Pin Names	Description
A, B	Input
Y	Output
NC	No Connect

Function Table

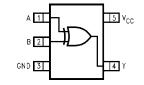
$$\mathbf{Y} = \mathbf{A} \oplus \mathbf{B}$$

Inp	uts	Output			
Α	В	Y			
L	L	L			
L	Н	Н			
Н	L	Н			
Н	Н	L			

H = HIGH Logic Level

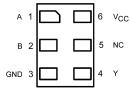
L = LOW Logic Level

Connection Diagrams Pin Assignments for SC70 and SOT23



(Top View)

Pad Assignment for MicroPak



(Top Thru View)

 $\label{eq:total_cond} \mbox{TinyLogio} \mbox{\mathbb{B} is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{\mathbb{M}}} \mbox{\mathbb{M} is a trademark of Fairchild Semiconductor Corporation.} \\$

Absolute Maximum Ratings(Note 1)

Supply Voltage (V $_{CC}$) \$-0.5V to +7.0V DC Input Diode Current (I $_{IK}$) \$=0.5V $-20~\rm{mA}$

 $@ \ V_{\text{IN}} \geq V_{\text{CC}} + 0.5 \text{V} \\ \text{DC Input Voltage } (V_{\text{IN}}) \\ & -0.5 \text{V to } V_{\text{CC}} + 0.5 \text{V} \\ \label{eq:power_powe$

DC Output Diode Current (I_{OK})

DC Output Source

or Sink Current (I_{OUT}) $\pm 12.5 \text{ mA}$

DC $\rm V_{\rm CC}$ or Ground Current

per Output Pin (I $_{\rm CC}$ or I $_{\rm GND}$) ± 25 mA Storage Temperature (T $_{\rm STG}$) $-65^{\circ}{\rm C}$ to $+150^{\circ}{\rm C}$

Junction Temperature (T_J) 150°C

Lead Temperature (T_L);

(Soldering, 10 seconds) 260°C

Power Dissipation (P_D) @ +85°C

SOT23-5 200 mW SC70-5 150 mW

Recommended Operating Conditions (Note 2)

Input Rise and Fall Time (t_r, t_f)

 V_{CC} @ 2.0V
 0 to 1000 ns

 V_{CC} @ 3.0V
 0 to 750 ns

 V_{CC} @ 4.5V
 0 to 500 ns

 V_{CC} @ 6.0V
 0 to 400 ns

Thermal Resistance (θ_{JA})

SOT23-5 300°C/W SC70-5 425°C/W

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

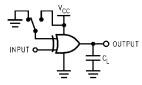
Symbol	Parameter	v _{cc}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
Cyllibol		(V)	Min	Тур	Max	Min	Max	Oilles	
V _{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V	
		3.0-6.0	$0.7 \mathrm{V_{CC}}$			0.7 V _{CC}		V	
V _{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V	
		3.0-6.0			$0.3\mathrm{V}_{\mathrm{CC}}$		$0.3\mathrm{V}_{\mathrm{CC}}$	V	
V _{OH}	HIGH Level Output Voltage	2.0	1.90	2.0		1.90			
		3.0	2.90	3.0		2.90		V	$I_{OH} = -20 \mu A$ $V_{IN} = V_{IH}, V_{IL}$
		4.5	4.40	4.5		4.40		V	$V_{IN} = V_{IH}, V_{IL}$
		6.0	5.90	6.0		5.90			
									$V_{IN} = V_{IH}, V_{IL}$
		3.0	2.68	2.85		2.63		V	$I_{OH} = -1.3 \text{ mA}$
		4.5	4.18	4.35		4.13		V	$I_{OH} = -2 \text{ mA}$
		6.0	5.68	5.85		5.63			$I_{OH} = -2.6 \text{ mA}$
V _{OL}	LOW Level Output Voltage	2.0		0.0	0.10		0.10		
		3.0		0.0	0.10		0.10	V	$I_{OL} = 20 \mu A$ $V_{IN} = V_{IH} \text{ or } V_{IL}$
		4.5		0.0	0.10		0.10	V	$V_{IN} = V_{IH}$ or V_{IL}
		6.0		0.0	0.10		0.10		
									$V_{IN} = V_{IH}$ or V_{IL}
		3.0		0.1	0.26		0.33	V	$I_{OL} = 1.3 \text{ mA}$
		4.5		0.1	0.26		0.33	•	$I_{OL} = 2 \text{ mA}$
		6.0		0.1	0.26		0.33		I _{OL} = 2.6 mA
I _{IN}	Input Leakage Current	6.0			±0.1		±1.0	μΑ	$V_{IN} = V_{CC}$, GND
I _{CC}	Quiescent Supply Current	6.0			1.0		10.0	μΑ	$V_{IN} = V_{CC}$, GND

AC Electrical Characteristics

Symbol	Parameter	V _{CC}	$T_A = +25^{\circ}C$			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure	
	, arameter	(V)	Min	Тур	Max	Min	Max	Units	Contantions	Number	
t _{PLH} ,	Propagation Delay	5.0		4.5	17			ns	$C_L = 15 pF$		
t_{PHL}		2.0		22	100		125			7_	
		3.0		12	27		35	200	C _I = 50 pF	Figures 1, 3	
		4.5		8.5	20		25	ns	OL = 50 pr		
		6.0		7	17		21				
t _{TLH} ,	Output Transition Time	5.0		3	8			ns	C _L = 15 pF		
t_{THL}		2.0		25	125		155			1	
		3.0		16	35		45	200	C = 50 pE	Figures 1, 3	
		4.5		11	25		31	ns	$C_L = 50 pF$., 0	
		6.0		9	21		26				
C _{IN}	Input Capacitance	Open		2	10		10	pF			
C _{PD}	Power Dissipation Capacitance	5.0		8				pF	(Note 3)	Figure 2	

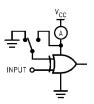
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static).

AC Loading and Waveforms



 $\mathrm{C_L}$ includes load and stray capacitance Input PRR = 1.0 MHz; $\mathrm{t_W} = 500~\mathrm{ns}$

FIGURE 1. AC Test Circuit



Input = AC Waveform;

PRR = variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

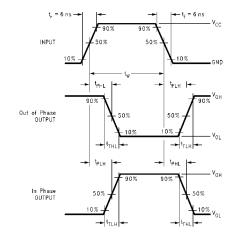


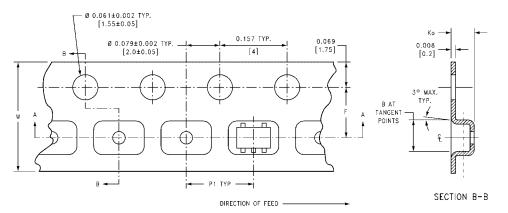
FIGURE 3. AC Waveforms

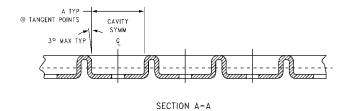
Tape and Reel Specification

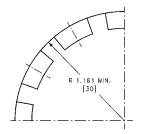
TAPE FORMAT for SC70 and SOT23

Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
M5X, P5X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

TAPE DIMENSIONS inches (millimeters)



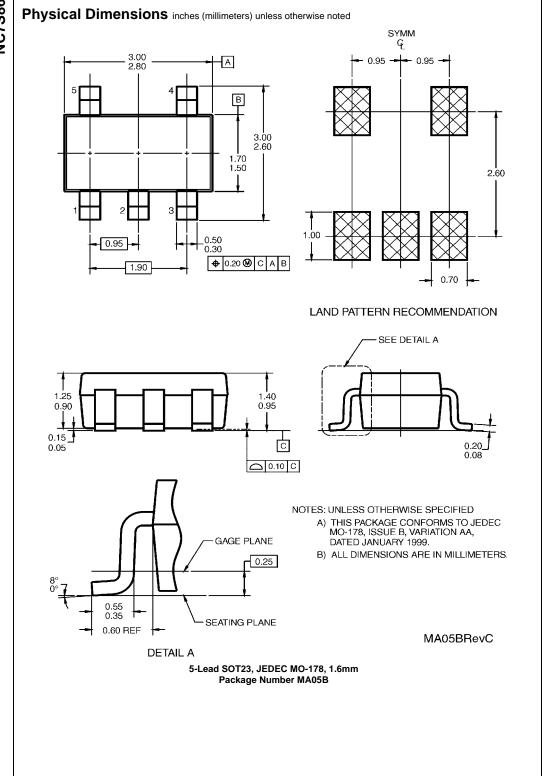


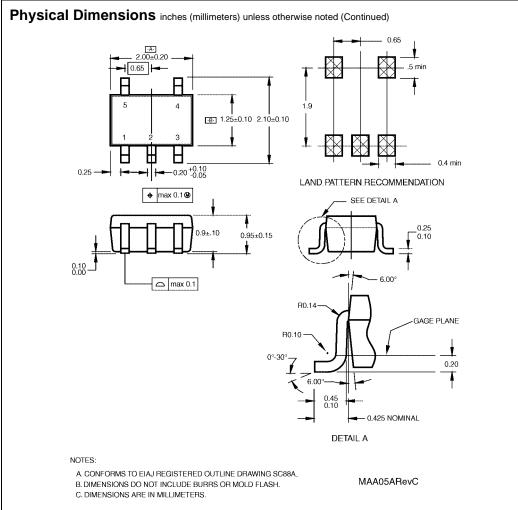


BEND RADIUS NOT TO SCALE

Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-5	8 mm	0.093	0.096	0.138 ±0.004	0.053 ±0.004	0.157	0.315 ±0.004
		(2.35)	(2.45)	(3.5 ±0.10)	(1.35 ±0.10)	(4)	(8 ±0.1)
SOT23-5	8 mm	0.130	0.130	0.138 ±0.002	0.055 ±0.004	0.157	0.315 ±0.012
		(3.3)	(3.3)	(3.5 ±0.05)	(1.4 ±0.11)	(4)	(8 ±0.3)

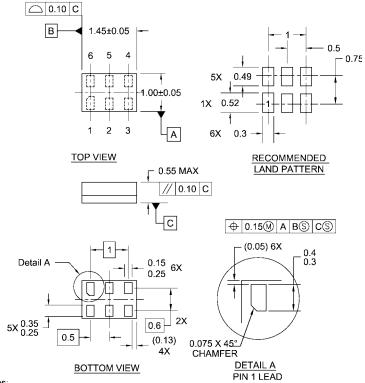
Tape and Reel Specification (Continued) TAPE FORMAT for MicroPak Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) 125 (typ) Empty Sealed L6X Carrier 5000 Filled Sealed Trailer (Hub End) 75 (typ) **Empty** Sealed 2.00-1.75±0.10 В 8.00 ^{+0.30} -0.10 3.50±0.05 1.15±0.05 **-** → В◄ -ø 0.50 ±0.05 SECTION B-B DIRECTION OF FEED SCALE:10X 0.254±0.020 Г 0.70±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X **DETAIL X** SCALE: 3X Tape Α В С D N W1 W2 W3 Size 0.331 +0.059/-0.000 0.567 W1 +0.078/-0.039 0.059 0.512 0.795 2.165 8 mm (177.8)(1.50)(13.00)(20.20)(55.00)(8.40 +1.50/-0.00) (14.40)(W1 +2.00/-1.00)





5-Lead SC70, EIAJ SC-88a, 1.25mm Wide Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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