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September 2014

FDMC2674

N-Channel UltraFET Trench MOSFET

220V, **7.0A**, **366m** Ω

Features

- Max $r_{DS(on)} = 366m\Omega$ at $V_{GS} = 10V$, $I_D = 1.0A$
- Typ $Q_q = 12.7$ nC at $V_{GS} = 10$ V
- Low Miller charge
- Low Q_{rr} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

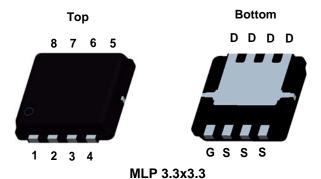


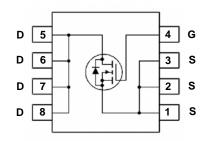
General Description

UltraFET device combines characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Application

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{DS}	Drain to Source Voltage			220	V
V _{GS}	Gate to Source Voltage			±20	V
I _D	Drain Current -Continuous (Silicon limited)	T _C = 25°C		7.0	
	-Continuous	T _A = 25°C	(Note 1b)	1.0	Α
	-Pulsed			13.8	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	11	mJ
D	Power Dissipation	T _C = 25°C		42	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.1	VV
T _J , T _{STG}	Operating and Storage Junction Temperature R	ange		-55 to +150	°C

Thermal Characteristics

R	BJC	Thermal Resistance, Junction to Case	(Note 1)	3.0	°C/W
R	^k eJA	Thermal Resistance, Junction to Ambient	(Note 1a)	60	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2674	FDMC2674	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units			
Off Characteristics									
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	220			V			
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		248		mV/°C			
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 176V, V _{GS} = 0V			1	μΑ			
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA			

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	3.4	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-10.2		mV/°C
r	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 1.0A$		305	366	mΩ
r _{DS(on)}		$V_{GS} = 10V, I_D = 1.0A, T_J = 150$ °C		678	814	11122

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 100V, V _{GS} = 0V, f = 1MHz	880	1180	pF
C _{oss}	Output Capacitance		70	95	pF
C _{rss}	Reverse Transfer Capacitance	1 – 110112	11	20	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		9	18	ns
t _r	Rise Time	$V_{DD} = 100V, I_{D} = 1.0A$ $V_{GS} = 10V, R_{GEN} = 2.4\Omega$	13	23	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GEN} = 2.452$	15	27	ns
t _f	Fall Time		21	34	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$ $V_{DD} = 15V$	12.7	18	nC
Q_{gs}	Gate to Source Gate Charge	I _D = 1.0A	3.8		nC
Q _{qd}	Gate to Drain "Miller" Charge		2.9		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 2.2A$ (Note 2)	0.8	1.5	V
t _{rr}	Reverse Recovery Time	-I _F = 1.0A, di/dt = 100A/μs		60	ns
Q_{rr}	Reverse Recovery Charge			109	nC

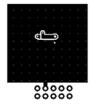
Notes:

1: R_{BJA} is determined with the device mounted on a 1 in² oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BJA} is determined by the user's board design.

(a)R_{BJA} = 60°C/M when mounted on a 1 in² pad of 2 oz copper, 1.5'x1.5'x0.062' thick PCB.

(b)R_{BJA} = 135°C/M when mounted on a minimum pad of 2 oz copper.





a. 60°C/W when mounted on a 1 in² pad of 2 oz copper



b. 135°C/W when mounted on a minimum pad of 2 oz copper

- 2: Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%. 3: Starting T $_J$ = 25°C; N-ch: L = 1mH, I $_{AS}$ = 4.7A, V $_{DD}$ = 25V, V $_{GS}$ = 10V.

Typical Characteristics T_J = 25°C unless otherwise noted

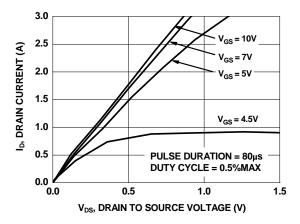


Figure 1. On-Region Characteristics

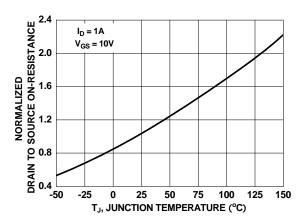


Figure 3. Normalized On-Resistance vs Junction Temperature

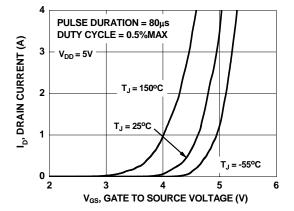


Figure 5. Transfer Characteristics

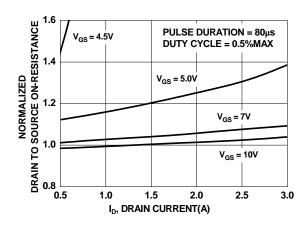


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

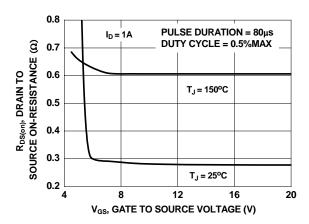


Figure 4. On-Resistance vs Gate to Source Voltage

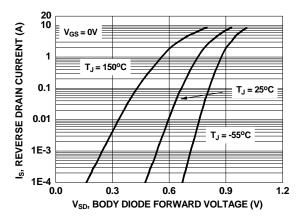


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

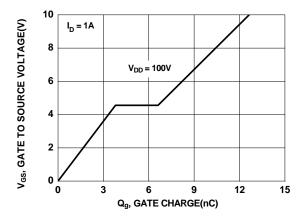


Figure 7. Gate Charge Characteristics

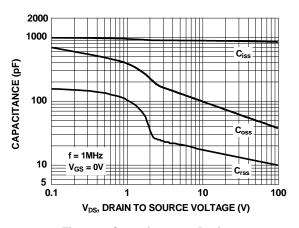


Figure 8. Capacitance vs Drain to Source Voltage

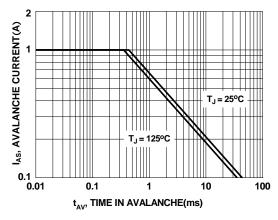


Figure 9. Unclamped Inductive Switching Capability

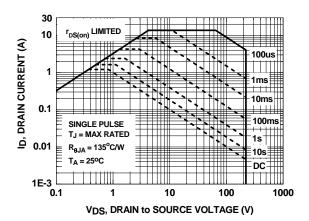


Figure 10. Forward Bias Safe Operating Area

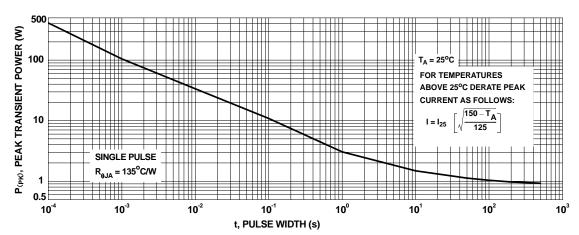


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

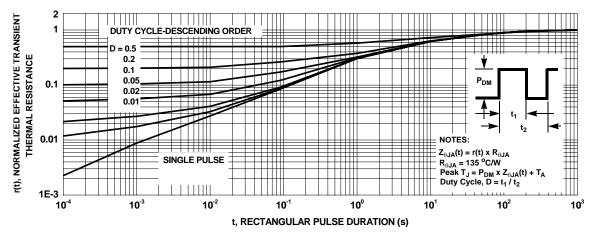
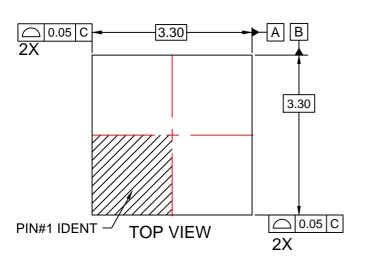
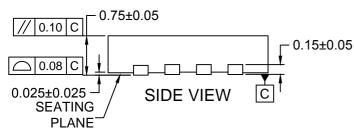
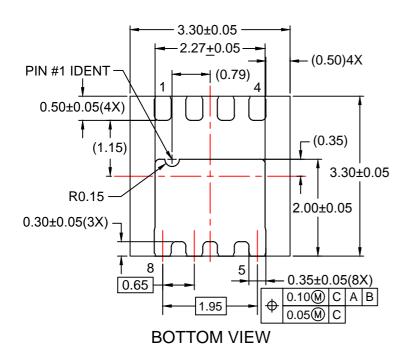
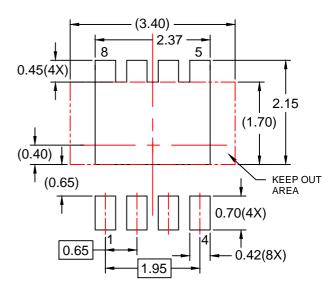


Figure 12. Transient Thermal Response Curve









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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