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November 2013

FQP20N06

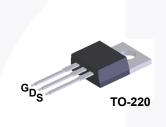
N-Channel QFET[®] MOSFET 60 V, 20 A, 60 m Ω

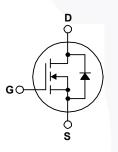
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 20 A, 60 V, $R_{DS(on)}$ = 60 m Ω (Max.) @ V_{GS} = 10 V, I_D = 10 A
- Low Gate Charge (Typ. 11.5 nC)
- Low Crss (Typ. 25 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings T_c = 25°C unless otherwise noted.

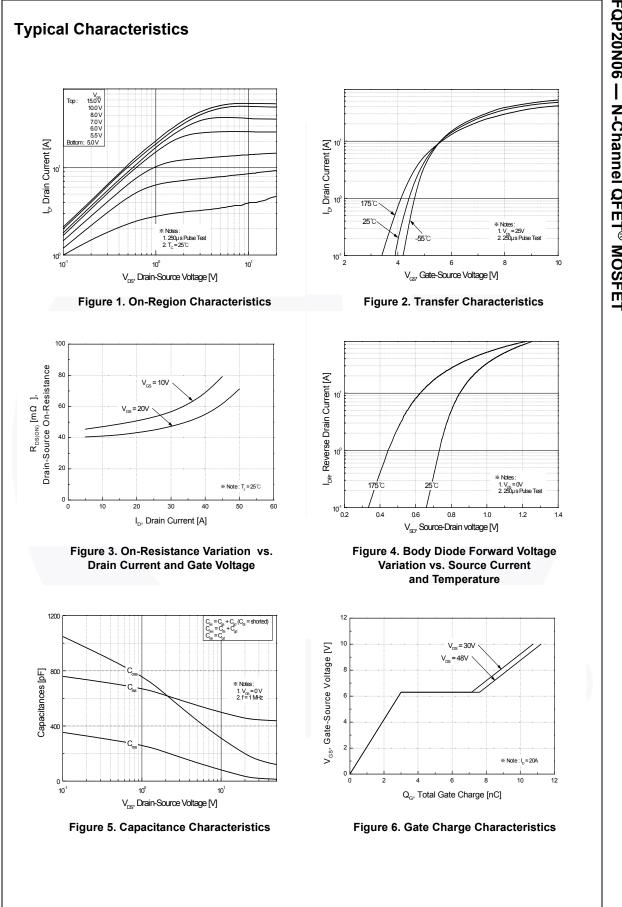
Symbol	Parameter		FQP20N06	Unit
V _{DSS}	Drain-Source Voltage		60	V
I _D	Drain Current - Continuous (T _C = 25°	°C)	20	A
	- Continuous (T _C = 100	0°C)	14.1	A
I _{DM}	Drain Current - Pulsed	(Note 1)	80	A
V _{GSS}	Gate-Source Voltage		± 25	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	155	mJ
I _{AR}	Avalanche Current	(Note 1)	20	A
E _{AR}	Repetitive Avalanche Energy	(Note 1)	5.3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
PD	Power Dissipation ($T_C = 25^{\circ}C$)		53	W
	- Derate above 25°C		0.35	W/°C
T _J , T _{STG}	Operating and Storage Temperature Rai	nge	-55 to +175	°C
TL	Maximum Lead Temperature for Solderin 1/8" from Case for 5 seconds	ng,	300	°C

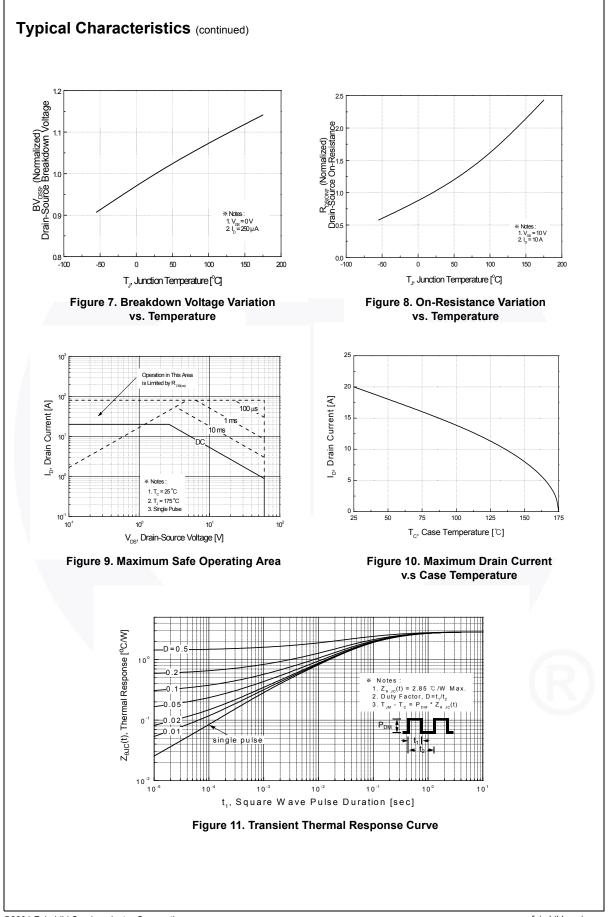
Thermal Characteristics

Symbol	Parameter	FQP20N06	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.85	°C/W	
R_{\thetaJA}	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

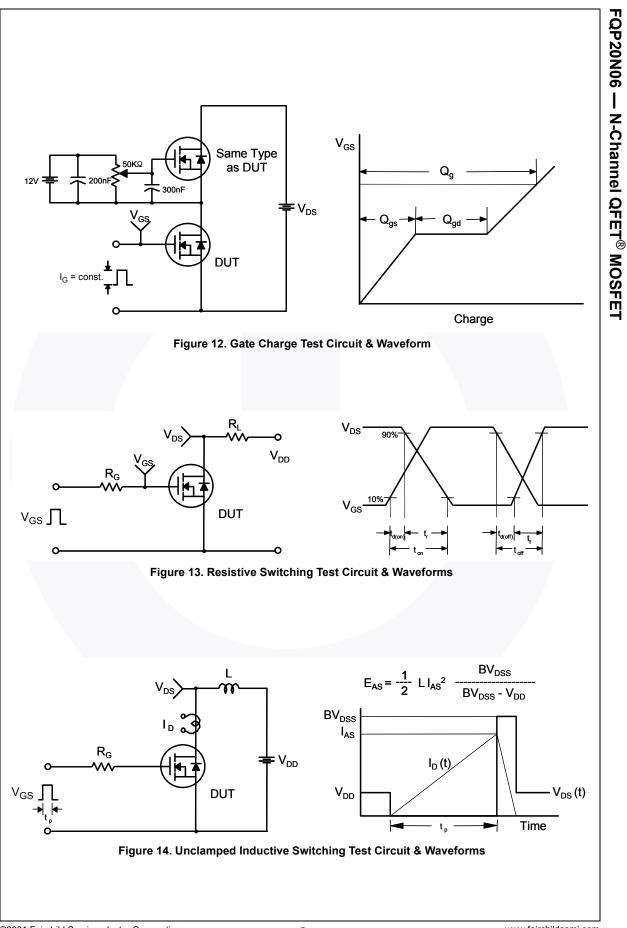
Part NumberTop MarkPackageFQP20N06FQP20N06TO-220		Package	Packing Method Reel S		e Tape Width		h Q	n Quantity	
		Tube N/A		N/A		5	50 units		
lectri	cal Cl	naracteristics	T _C = 25°C	unless otherwise noted.					
Symbol		Parameter		Test Condit	ions	Min	Тур	Max	Unit
Off Cha	aractor	ietice							
V _{DSS}		Source Breakdown V	oltage	V _{GS} = 0 V, I _D = 250 J	A	60			V
BV _{DSS}		lown Voltage Temper	U			00			v
ΔT_{J}	Coeffic	•	alure	$I_D = 250 \ \mu A$, Referen	nced to 25°C		0.07		V/°C
DSS	7	Nata Malta na Drain G		V_{DS} = 60 V, V_{GS} = 0	V			1	μA
	Zero G	Sate Voltage Drain Cu	Irrent	V _{DS} = 48 V, T _C = 15	0°C			10	μA
GSSF	Gate-E	Body Leakage Currer	t, Forward	V_{GS} = 25 V, V_{DS} = 0	V			100	nA
SSSR	Gate-E	Body Leakage Curren	it, Reverse	V_{GS} = -25 V, V_{DS} = (V			-100	nA
On Cha	aracter	istics							
GS(th)	1	hreshold Voltage		V _{DS} = V _{GS} , I _D = 250	μA	2.0		4.0	V
CS(in)	Static	Drain-Source		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	r.		0.048	0.06	Ω
FS		sistance rd Transconductance		V _{DS} = 25 V, I _D = 10 /	^		12		S
-		racteristics					450	500	
viss	-	Capacitance		V _{DS} = 25 V, V _{GS} = 0	V,		450	590	pF
YOSS		Capacitance		f = 1.0 MHz			170	220	pF
rss	Revers	se Transfer Capacitar	nce				25	35	pF
Switch	ing Ch	aracteristics							
l(on)	Turn-C	n Delay Time		$V_{} = 30 V I_{-} = 10$	Δ		5	20	ns
	Turn-C	In Rise Time		$V_{DD} = 30 \text{ V}, \text{ I}_{D} = 10 \text{ A},$ R _G = 25 Ω			45	100	ns
l(off)	Turn-C	off Delay Time		NG 2012			20	50	ns
. ,	Turn-C	Off Fall Time			(Note 4)		25	60	ns
) _a	Total C	Gate Charge		V _{DS} = 48 V, I _D = 20 /	۹.		11.5	15	nC
l _{gs}	Gate-S	Source Charge		$V_{GS} = 10 V$			3		nC
gd gd	Gate-E	Drain Charge		66	(Note 4)		4.5		nC
			ļ						
				d Maximum Rat	ings				
8		um Continuous Drair						20	A
SM		um Pulsed Drain-Sou	1					80	A
SD		Source Diode Forwar	d Voltage	$V_{GS} = 0 V, I_S = 20 A$				1.5	V
r		se Recovery Time		$V_{GS} = 0 V, I_{S} = 20 A,$			43		ns
۱, rr	Revers	se Recovery Charge		dI _F / dt = 100 A/µs			50		nC

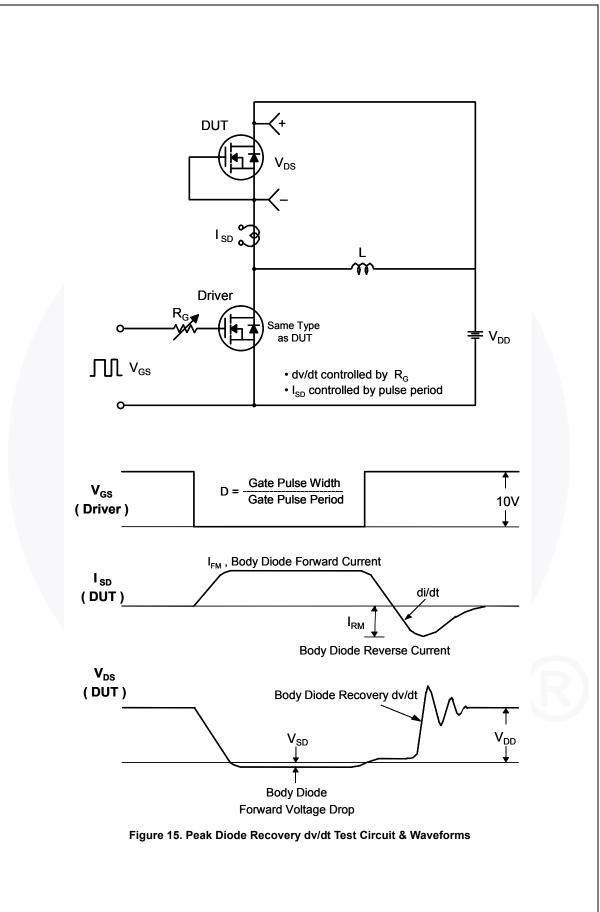
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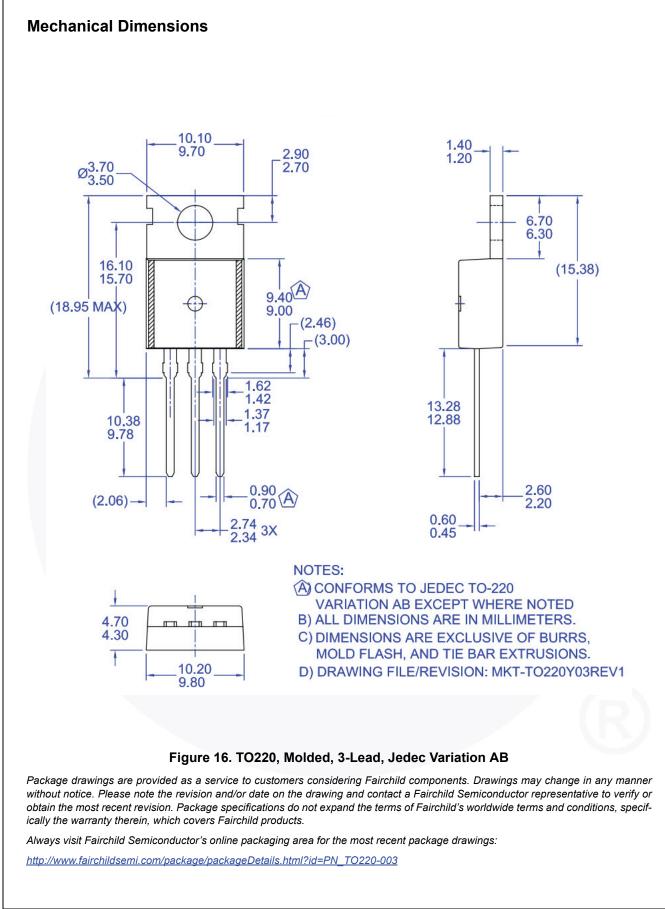


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